Modelling Power Consumption of the Intel SCC

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Overview

- Introduction
- Power management features of the Single Chip Cloud computer
- Power consumption Model (algorithmic level)
- Experiments
- Conclusions
Introduction

- Energy consumption by computers is continuously growing → green computing gains more interest

- Intel Single-chip Cloud Computer (SCC) supports energy efficient computing

- There are a lot of algorithmic-level techniques for energy-efficient computing → parameterized model

- Derive the models‘ parameters for the SCC by measuring the power consumption and compare it to the power model with a least-scares error analysis
Power Management features of the SCC I

- 48 independent cores organized in 24 tiles
- Tiles are linked together through an on-chip network
- 4 Memory controllers
Power Management features of the SCC I

- Cores are organized in 24 frequency islands and 6 voltage islands
- Network and memory controllers are frequency islands of their own
Power Management features of the SCC II

- RCCE Library offers power management functions to change frequency and voltage during runtime.

- Possibilities:
  - Change frequency and voltage of different islands separately.
  - Change frequency and let voltage automatically scale to lowest stable state.

→ In this case: There are only 6 power domains.
Power Management features of the SCC III

- One can vary the frequency (and voltage) as depicted in the following table

<table>
<thead>
<tr>
<th>Tile Frequency (MHz)</th>
<th>RCCE Frequency Divider</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>800</td>
<td>2</td>
<td>1.1</td>
</tr>
<tr>
<td>533</td>
<td>3</td>
<td>0.8</td>
</tr>
<tr>
<td>400</td>
<td>4</td>
<td>0.7</td>
</tr>
<tr>
<td>320</td>
<td>5</td>
<td>0.7</td>
</tr>
<tr>
<td>266</td>
<td>6</td>
<td>0.7</td>
</tr>
<tr>
<td>228</td>
<td>7</td>
<td>0.7</td>
</tr>
<tr>
<td>200</td>
<td>8</td>
<td>0.7</td>
</tr>
<tr>
<td>178</td>
<td>9</td>
<td>0.7</td>
</tr>
<tr>
<td>160</td>
<td>10</td>
<td>0.7</td>
</tr>
<tr>
<td>145</td>
<td>11</td>
<td>0.7</td>
</tr>
<tr>
<td>133</td>
<td>12</td>
<td>0.7</td>
</tr>
<tr>
<td>123</td>
<td>13</td>
<td>0.7</td>
</tr>
<tr>
<td>114</td>
<td>14</td>
<td>0.7</td>
</tr>
<tr>
<td>106</td>
<td>15</td>
<td>0.7</td>
</tr>
<tr>
<td>100</td>
<td>16</td>
<td>0.7</td>
</tr>
</tbody>
</table>
Abstract level:

Dynamic power consumption of a semiconductor device at frequency $f$ (with fixed supply voltage) is

$$p_{dyn}(f) = b \cdot f^a$$

It also has a frequency-independent static power consumption $p_{stat} = s$

Then, the total power consumption is

$$p(f) = p_{dyn}(f) + p_{stat} = b \cdot f^a + s$$
Abstract level:
As the static power consumption is linear in the supply voltage and as the minimum possible supply voltage for a given frequency on SCC can be approximated by a linear relationship, we get

\[ p(f) = p_{\text{dyn}}(f) + p_{\text{stat}} = b \cdot f^a + s \cdot f \]
Power Consumption Model III

- Referred to the SCC:
  If 6 power domains (frequencies $f_1$ to $f_6$) and the on-chip network (frequency $f_0$)

\[
p_{acc}(f_0, \ldots, f_6) = p_n(f_0) + p_m + \sum_{i=1}^{6} 8 \cdot p_c(f_i)
\]

\[
= b_n \cdot f_0^{a_n} + 8 \cdot \sum_{i=1}^{6} b_c \cdot f_i^{a_c} + s_n \cdot f_0 + s_m + 8 \cdot \sum_{i=1}^{6} s_c \cdot f_i
\]
Power Consumption Model III

- Referred to the SCC:
  We did not vary the network frequency $f_0$. → the term $p_n(f_0)$ can also be considered static

This results in the following equation:

$$p_{scc}(f_1, \ldots, f_6) = 8 \cdot \sum_{i=1}^{6} (b_c \cdot f_i^a + s_c \cdot f_i) + \tilde{s}$$

where $\tilde{s} = p_n(f_0) + s_m$
Experiments I

- The experiments are designed to derive the numerical values of $b_c$, $s_c$ and $\tilde{s}$. The value $a_c$ is fixed to $a_c = 3$.

- Cores are split into two groups of size $8k$ and $48 - 8k$ each ($k = 0, \ldots, 6$).

- One group has a higher freq. (800, 533 or 400 MHz), the other group a lower freq. (200 or 100 MHz).
Experiments II

- Microbenchmark program: Execution can be divided into two steps:

  **Step 1:** Do some initialization. Change frequencies of the high- and low-freq. groups. Synchronize all cores by a barrier.

  **Step 2:** Simulate an expensive calculation (depending on user defined settings) within a time controlled loop for 10 seconds.
Experiments III

- Various benchmark settings, that differ in the use of caches, and intensity and regularity of memory access.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Step 1: One variable, initially set to 0</td>
</tr>
<tr>
<td></td>
<td>Step 2: Variable is incremented by 1</td>
</tr>
<tr>
<td>1</td>
<td>Step 1: array[size $10^6$], initially set to 0</td>
</tr>
<tr>
<td></td>
<td>Step 2: array elements added up successively</td>
</tr>
<tr>
<td>2</td>
<td>Step 1: array[size $10^6$], initially set to max_int</td>
</tr>
<tr>
<td></td>
<td>Step 2: array elements added up successively</td>
</tr>
<tr>
<td>3</td>
<td>Step 1: array[size $10^6$], initially set to index</td>
</tr>
<tr>
<td></td>
<td>Step 2: array elements added up in the following order:</td>
</tr>
<tr>
<td></td>
<td>$(7 \cdot \text{index} + \text{rank}) \mod \text{array_size}$</td>
</tr>
</tbody>
</table>
Experiments IV

- Power Consumption measurements:
  - every 10th ms within the loop → 1000 measurement points
  - each experiment is repeated five times
  - use the FPGA on the Rocky Lake Board to measure the power consumption
  - workload mostly varies in a range of 2 Watt and there are less than 5 outliers on each experiment
Results I

- Power consumption of the SCC for all microbenchmark settings with a different number of high-frequency domains
Results II

- Least-squares error analysis of equations:
  - insert the frequency values and a fixed value of 3 for $\alpha_c$
  - we obtain the values:
    \[
    b_c \approx 2.015 \cdot 10^{-9} \text{ Watt/MHz}^c \\
    s_c \approx 10^{-6} \text{ Watt/MHz} \\
    \tilde{s} \approx 23 \text{ Watt}
    \]

- Average error is 1.95 Watt (5.58%)

- Relative error ranges from -14.66% to 24.73%
Results III

Theoretical and measured power consumption

- Watt (measured)
- Watt (theoretical)
Conclusions

- Our research provides the SCC-specific parameters for power consumption models.
- Thus, we provide a link between the worlds of hardware and high-level algorithmics.
Future work

- include changes of the network frequency
- use insights to derive a power-optimal algorithmic mapping of streaming applications onto the Intel SCC
- extend the model to include situations where cores can be switched off completely
- refine the timing measurements to derive time penalties for changing voltage or frequency
Thanks a lot for your attention!